

Figure 1A

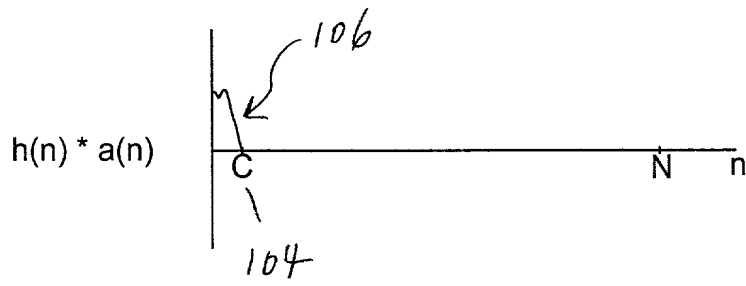


Figure 1B

200

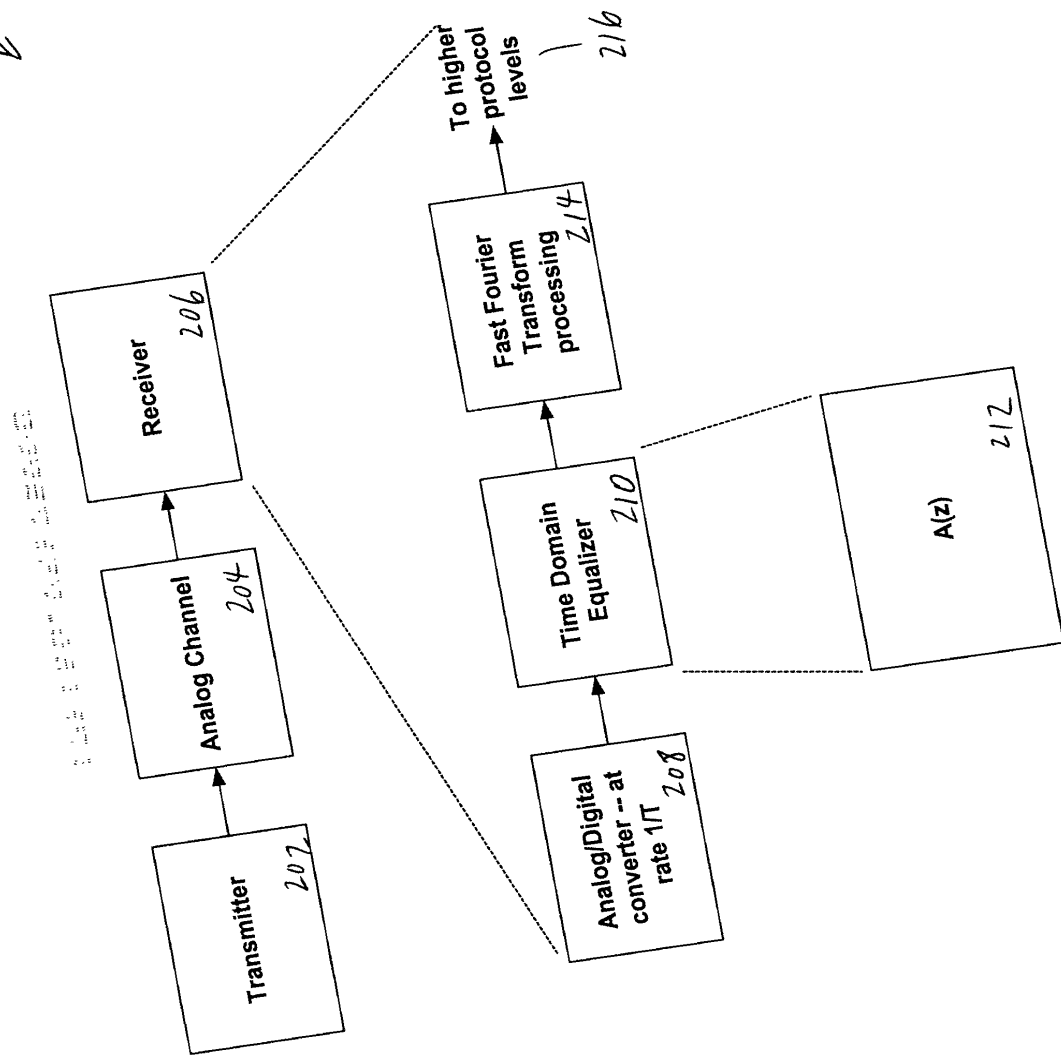


Figure 2

300

Figure 3 shows a block diagram of a system 300 for transmitting and receiving signals over a channel 303. The system includes a transmitter 301 and a receiver 309. The transmitter 301 receives an input signal $\delta(n)$ and processes it through a block $H(z)$ 302 to produce a signal $h(n)$. This signal $h(n)$ is then transmitted through the channel 303 to the receiver 309. The receiver 309 includes a block $A(z)$ 306 that receives $h(n)$ and produces a signal $h(n) * a(n)$. This signal is then processed by the FFT and higher layers of the ADSL receiver 318. The receiver 309 also includes a residual block $B(z)$ 306 that receives the input signal $\delta(n)$ and produces a signal $b(n)$. The signals $h(n) * a(n)$ and $b(n)$ are combined at a summing junction 308 to produce the error signal $e(n)$, which is then processed by the FFT and higher layers of the ADSL receiver 318. The error signal $e(n)$ is also fed back to the residual block $B(z)$ 306.

303

Channel

301

Transmitter

1

$\delta(n)$

$H(z)$

302

$H(z)$

$h(n)$

$A(z)$

306

$H(z)A(z)$

$h(n) * a(n)$

TEQ 304

318

FFT and higher layers of ADSL receiver

+

Σ

308

$E(z)$

$e(n)$

310

307

Residual

$B(z)$

306

$B(z)$

$b(n)$

Figure 3

General flow of steps

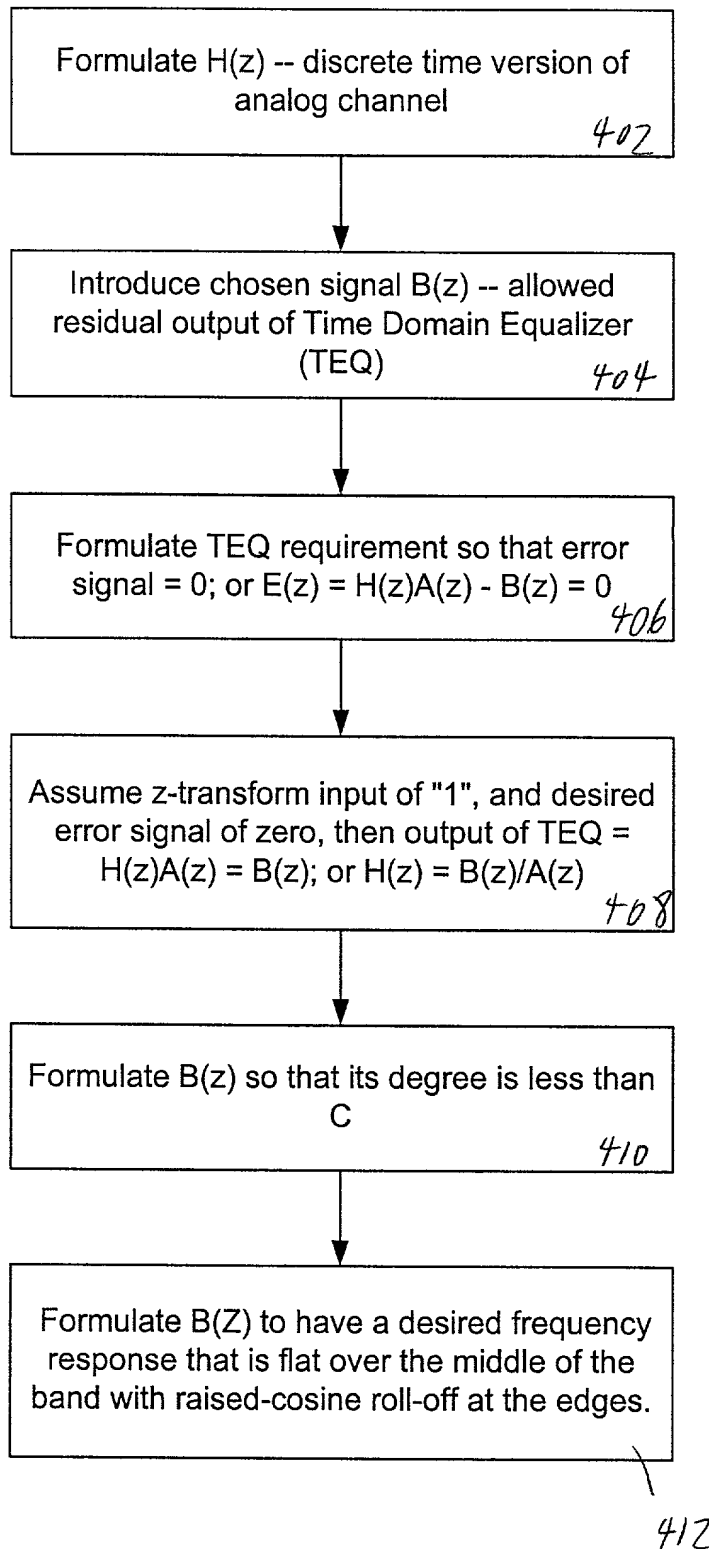


Figure 4

Formulate $B(z)$

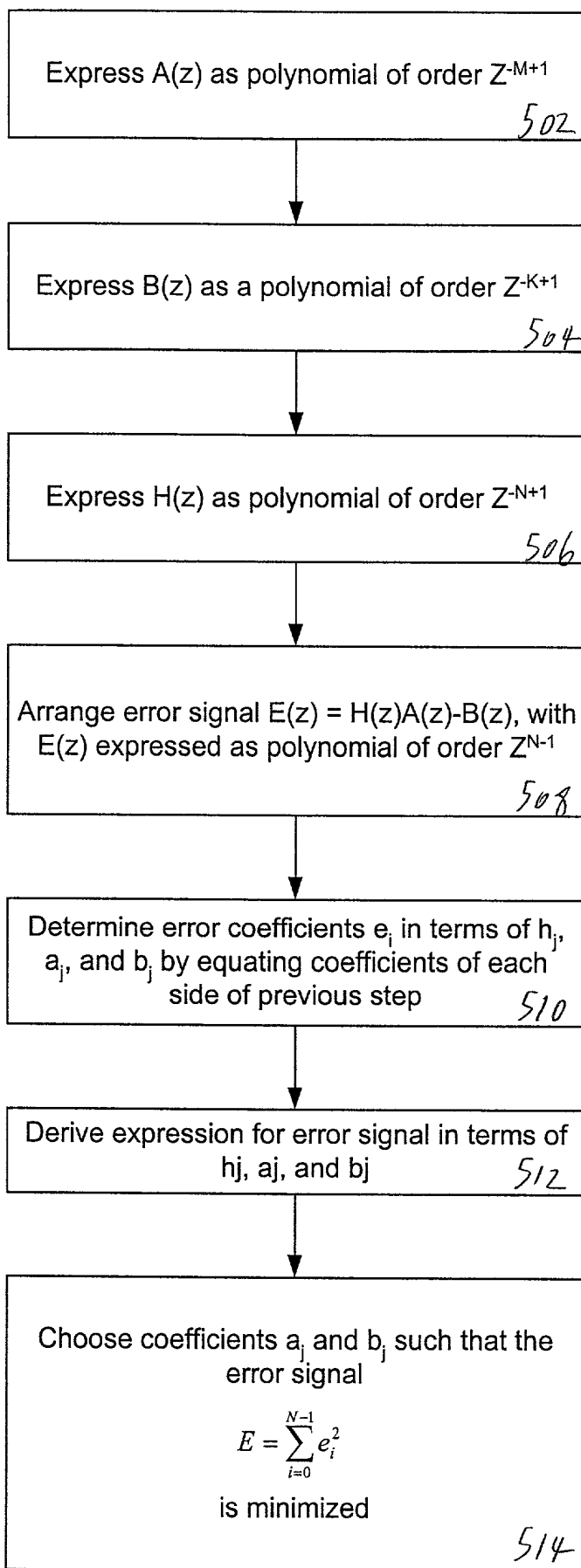


Figure 5

Minimize error signal

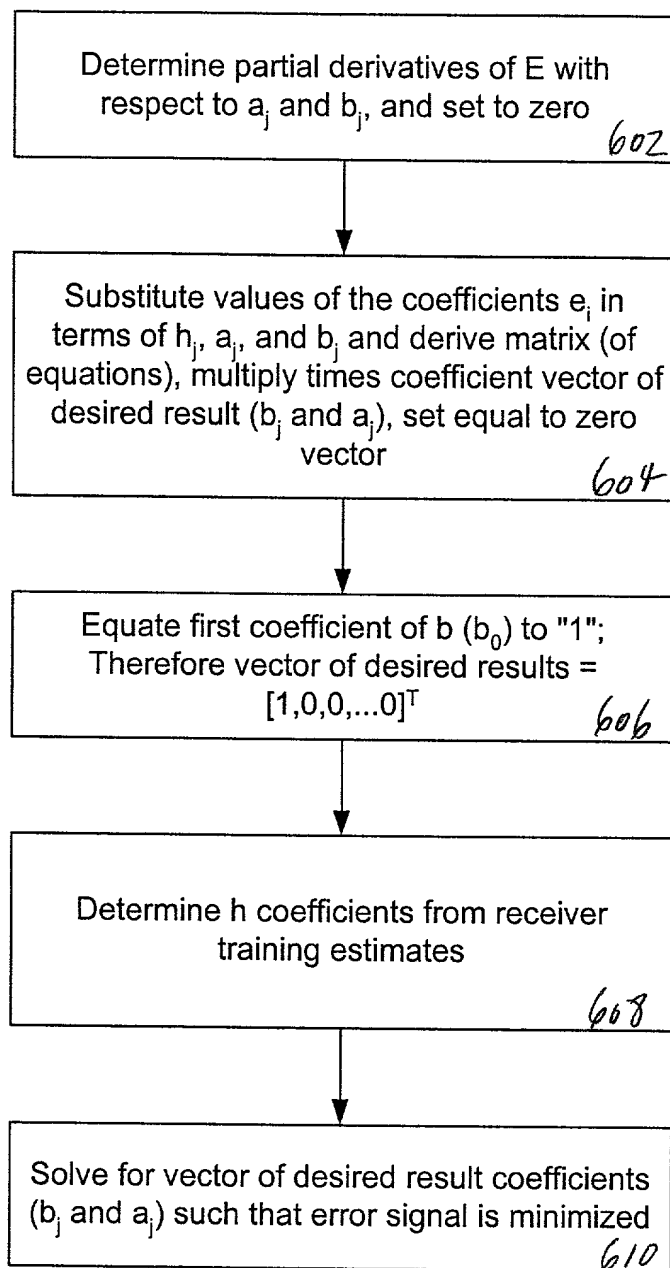


Figure 6